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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,319	11/26/2001	Tatsuya Takahashi	81784.0246	9511

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EXAMINER	
AGGARWAL, YOGESH K	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,319	TAKAHASHI, TATSUYA	
	Examiner	Art Unit	
	Yogesh K Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 November 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Horiguchi et al. (US PG-PUB # 2003/0058002).

[Claim 1]

Applicant's admitted prior art teaches a charge transfer device having a source follower amplification circuit (figure 1, element 8), wherein said source follower amplification circuit comprises an amplification transistor (figure 1, element Td1) which receives, at a gate, the voltage signal from said output section and outputs, from a source, an output signal corresponding to a change in the voltage signal (See figure 1, Paragraph 5); a load transistor (figure 1, element T_{L1}) connected between said amplification transistor (figure 1, element Td1) and a first power source (figure 1, element Vgb) for causing a constant current to flow from said amplification transistor to the side of the first power source (Paragraph 5). Applicant's admitted prior art fails to teach "a control transistor connected between said amplification transistor and a second power source, wherein said control transistor cuts off a current flowing from the second power source to said amplification transistor according to a control signal". However Horiguchi et al. teaches a transistor M_{C1} (figure 4) to be used as a control transistor connected between a power source (figure 4, V_{CC}) and a transistor Mp and when the gate voltage (phi $_C$) is brought to

a low level to the current is cut off (Paragraph 96) in order for the circuit to work in a low power consumption mode. Therefore taking the combined teachings of Applicant's admitted prior art and Horiguchi et al., it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have a control transistor connected between a transistor and a second power source, wherein the control transistor cuts off a current flowing from the second power source to the transistor according to a control signal. The benefit of doing so would be to reduce the power consumption as taught in Horiguchi (Paragraph 96).

[Claim 2]

Horiguchi teaches that the voltage potential phiC and phiS connected to the gates of transistors M_{C1} and M_{S1} are equal in magnitude (See figures 5A-C) which means that an input terminal is connected to a gate of the control transistor M_{C1} and to a gate of said load transistor M_{S1} commonly.

[Claim 3]

Horiguchi does not explicitly disclose a control signal generating provided between the gate of said control transistor and said input terminal for generating said control signal based on an input signal externally input to said input terminal. However, because the voltage potential phiC and phiS connected to the gates of transistors M_{C1} and M_{S1} are inverse of each other (Just like the applicant's specification in Paragraphs 50 and 51) as shown in figures 5A-C, Official Notice is taken of the fact that it is common to have a control signal generating circuit being provided for generating the inverse of a voltage signal to be connected between the gate of a control transistor and input terminal. Therefore taking the combined teachings of Horiguchi and Official Notice it would have been obvious to one skilled in the art at the time of the invention to have been

motivated to have a control signal generating circuit being provided for generating the inverse of a voltage signal to be connected between the gate of control transistor and input terminal in order to reduce the power consumption by controlling the current.

[Claim 4]

Horiguchi teaches that the control transistor is an enhancement type (Paragraph 96).

[Claim 5]

See claim 2.

[Claim 6]

See claim 3.

[Claims 7-12]

These claims correspond to claims 1-6. Therefore they are analyzed and rejected based upon claims 1-6 respectively.

3. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, Horiguchi et al. (US PG-PUB # 2003/0058002) in further view of Yonemoto (US Patent # 6,366,321).

[Claims 13 and 14]

Applicant's admitted prior art in view of Horiguchi teach means for reducing the current (Paragraph 96 of Horiguchi) but fail to teach "reducing a current flowing in the means for receiving and outputting during the period in which a pixel signal is not read out and though imaging is performed". However Yonemoto teaches at the end of the read-out period (i.e. during the period in which a pixel signal is not read out) and imaging is performed the drain current is reduced extremely (col. 12 lines 66-col. 13 line 3) in order to reduce the power consumption

(P=Vdd x Id). Therefore taking the combined teachings of Applicant's admitted prior art, Horiguchi et al. and Yonemoto, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to reduce a current flowing in the receiving and outputting during the period in which a pixel signal is not read out and though imaging is performed. The benefit of doing so would be to reduce the thermal noise as taught by Yonemoto (col. 13 lines 3-6).

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, Horiguchi et al. (US PG-PUB # 2003/0058002) in further view of Tonosaki et al. (US PG-PUB # 20020000950).

[Claim 15]

Applicant's admitted prior art in view of Horiguchi teach means for reducing the current (Paragraph 96 of Horiguchi) but fail to teach "reducing or increasing a current flowing in the means for receiving and outputting suitable for each image quality of imaging modes". However Tonosaki et al. teaches when the two-dimensional image is displayed in a third or fourth modes, the consumed current at the time of the use is reduced (Paragraph 13) in order to reduce the power consumption. Therefore taking the combined teachings of Applicant's admitted prior art, Horiguchi et al. and Tonosaki, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to reduce or increase a current flowing in the means for receiving and outputting suitable for each image quality of imaging modes. The benefit of doing so would be to reduce the power consumption.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K Aggarwal whose telephone number is (703) 305-0346. The examiner can normally be reached on M-F 9:00AM-5:30PM.

5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
October 12, 2004

TUAN HO
PRIMARY EXAMINER